

**Revision : 4.0**

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24	ATX, FRONT PANEL
25	VCORE (PWMISL6324+6612A)

[illegible]

**Model Name:GA-78LMT-S2P**

## Component value change history

Version: 4.0

**P-Code: U99098-0**

[illegible]

### Circuit or PCB layout change for next version

[illegible]

**GIGABYTE™**

Title	Author	Year	Journal	Volume	Page
1. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1-15
2. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	16-30
3. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	31-45
4. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	46-60
5. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	61-75
6. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	76-90
7. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	91-105
8. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	106-120
9. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	121-135
10. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	136-150

## BOM & PCB HISTORY

Size	
Customer	

Document Number

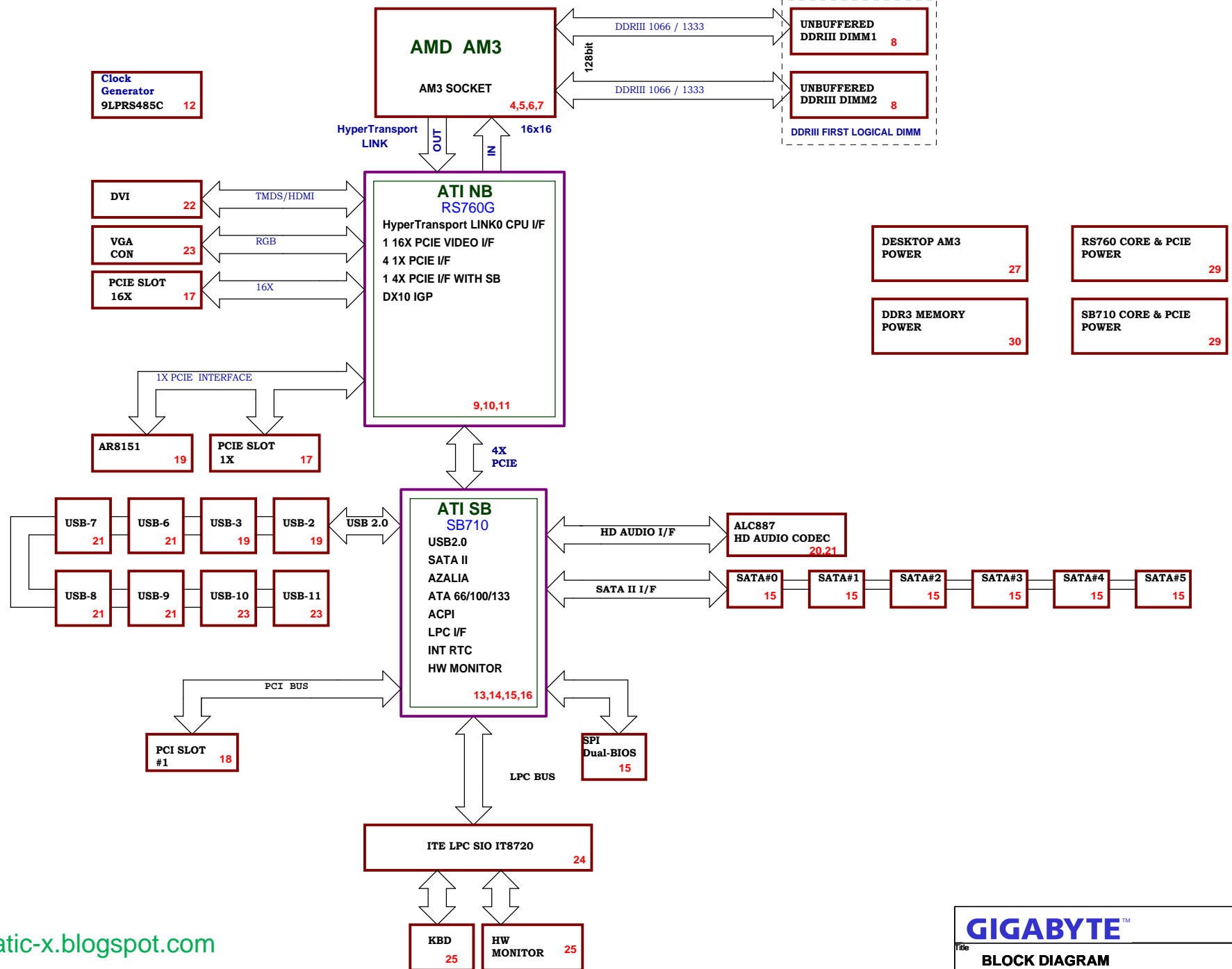
**GA-78LMT-S2P**

Rev  
4.0

Date: Friday, September 23, 2011

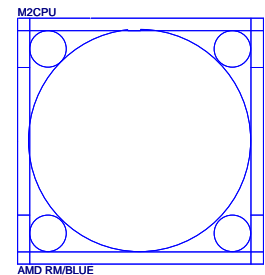
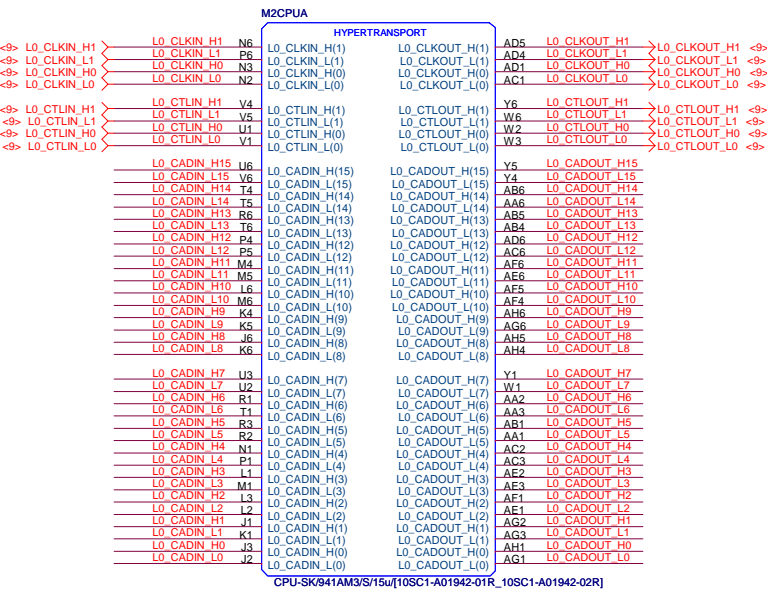
Sheet 2 of 28

# RS780L CUSTOMER DESKTOP DESIGN



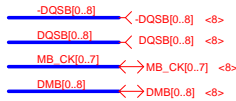
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L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] <9>

L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] <9>  
L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] <9>



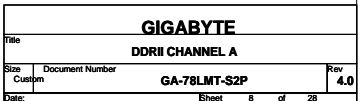
CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR18V  
CPU\_VTT\_SUS = DDRVTT

VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B







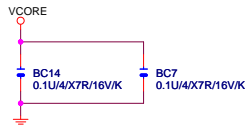
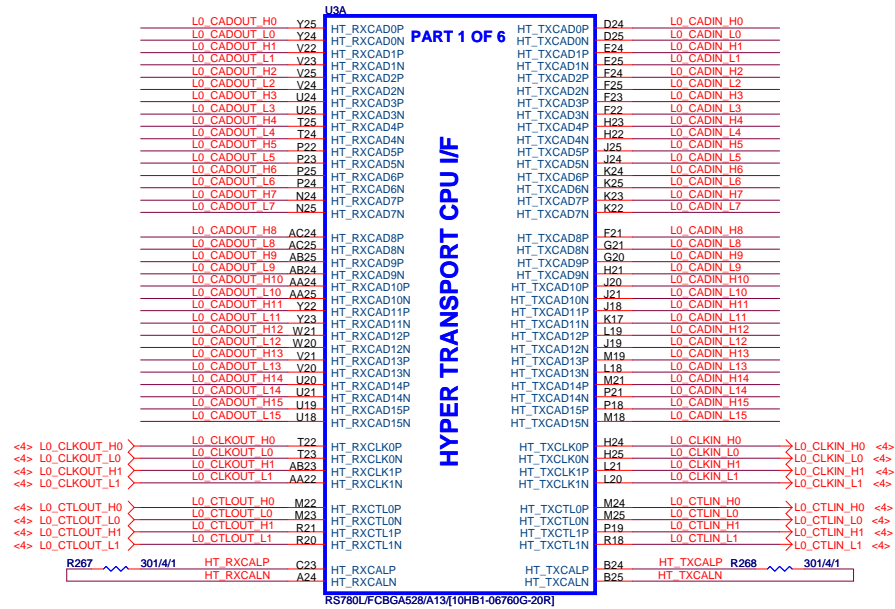




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L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] <4>  
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PART 1 OF 6

HYPER TRANSPORT CPU I/F



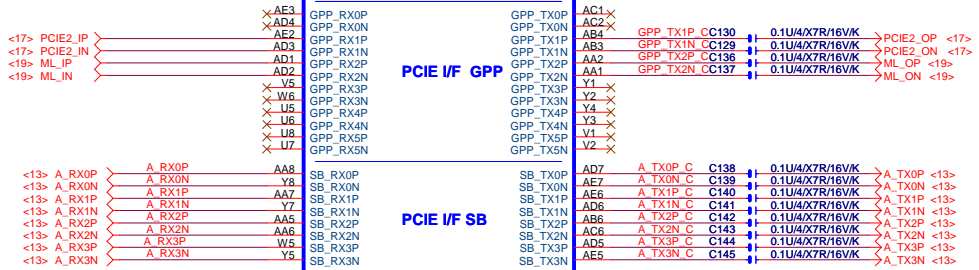
EXP\_A\_RXP[0..15] >>>EXP\_A\_RXP[0..15] <17>  
EXP\_A\_RXN[0..15] >>>EXP\_A\_RXN[0..15] <17>  
EXP\_A\_TXP[0..15] >>>EXP\_A\_TXP[0..15] <17>  
EXP\_A\_TXN[0..15] >>>EXP\_A\_TXN[0..15] <17>

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB



PCE\_CALRP(PCE\_BCALRP)  
PCE\_CALRN(PCE\_BCALRN)

RS780L/FCBGA528/A13[10HB1-06760G-20R]

NB\_HS[12SP2-SA0701-01R\_12SP2-SA0701-02R]

GIGABYTE™

RS780 HT-LINK I/F

Size Custom Document Number GA-78LMT-S2P Rev 4.0

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# RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX\_CAL, place close to pin C8

RS740\_DFT\_GPIO1 R272 150/4/1

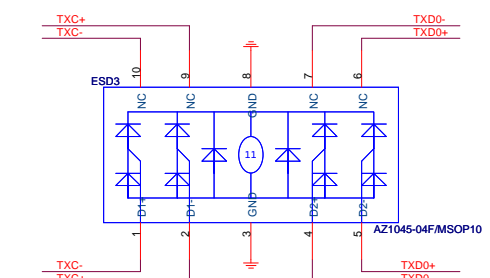
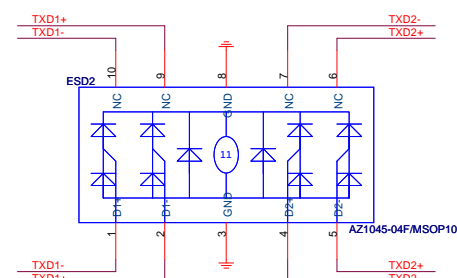
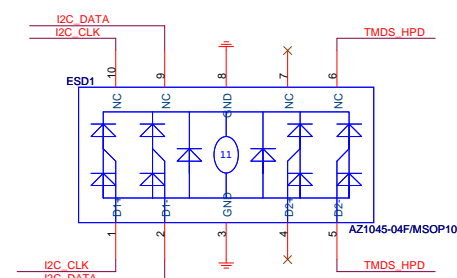
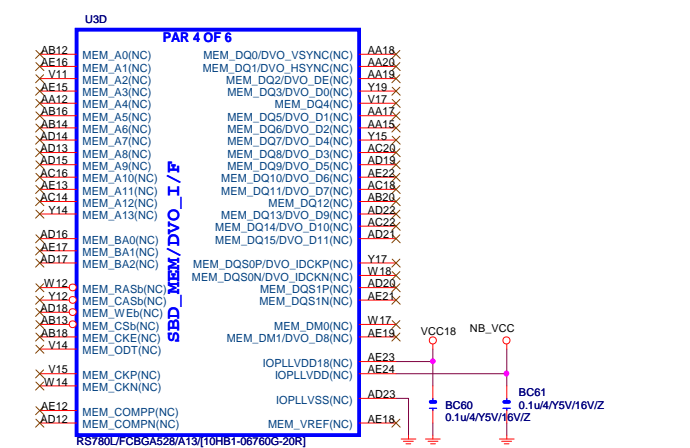
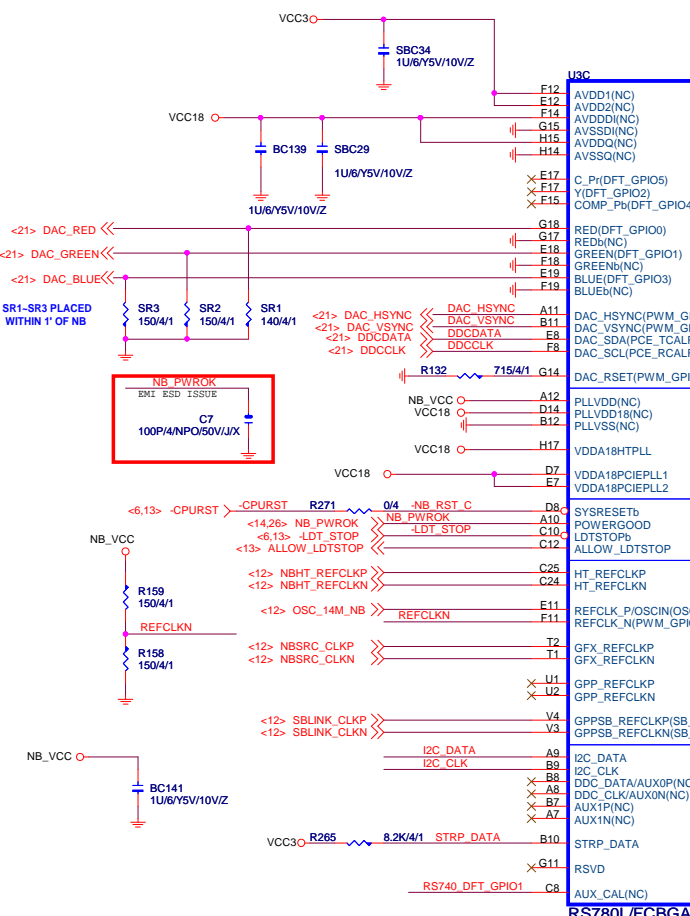
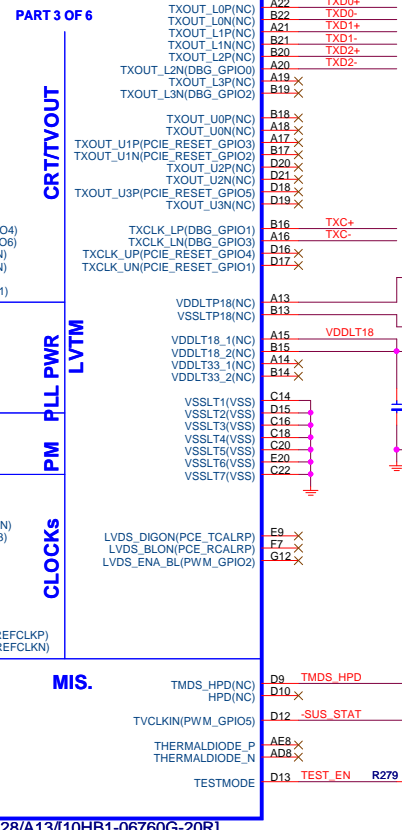
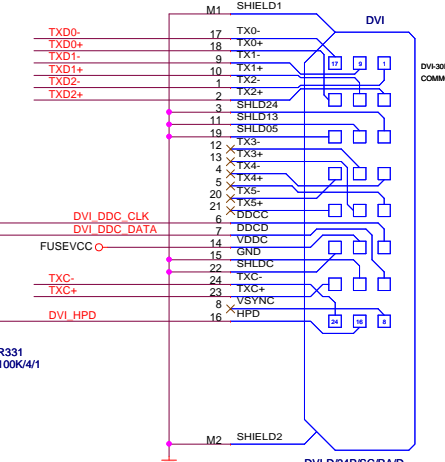
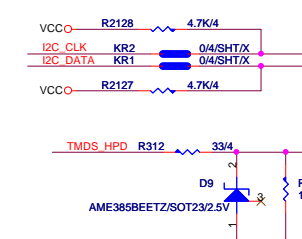
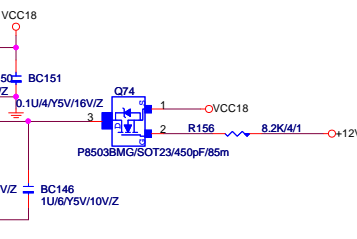
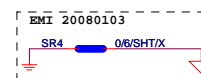
Note: for RX780, R217 (RX780\_DFT\_GPIO1) to 3K accordingly

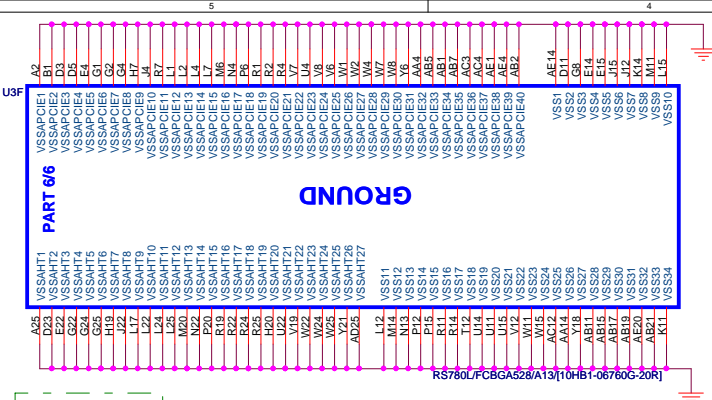
<21> DAC\_VSYNC << R276 3K/4/1 >> VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly  
R912 (RX780\_DFT\_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly  
R913 (RX780\_DFT\_GPIO4)  
R218 (RX780\_DFT\_GPIO3)  
R911 (RX780\_DFT\_GPIO2)

Note: for RX780, change following pull-down resistor to 3K accordingly  
R219 (RX780\_DFT\_GPIO0)

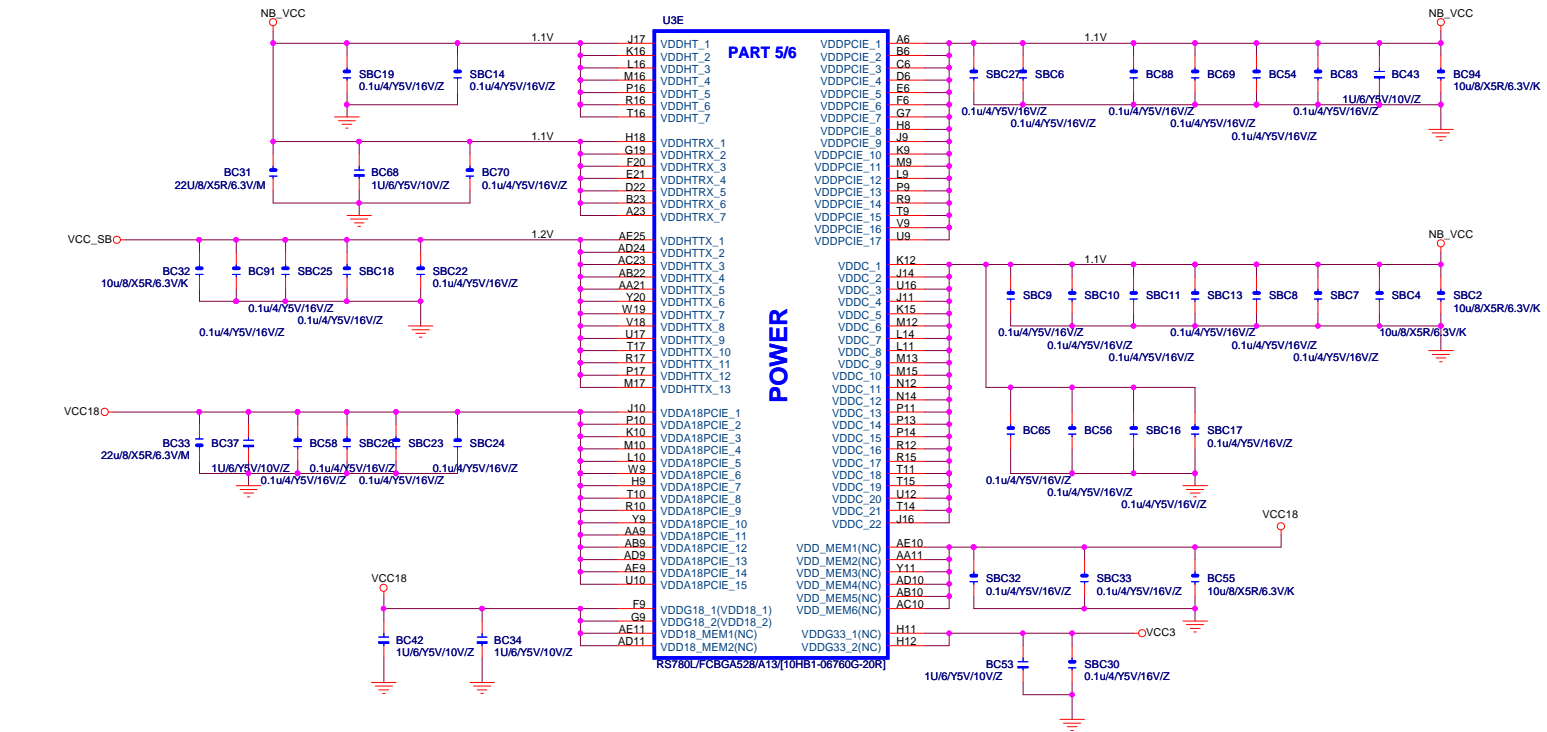


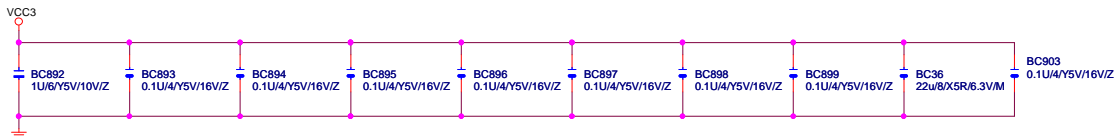


Please use 1mm pad size,  
place all ELT test pads  
on bottom side only

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



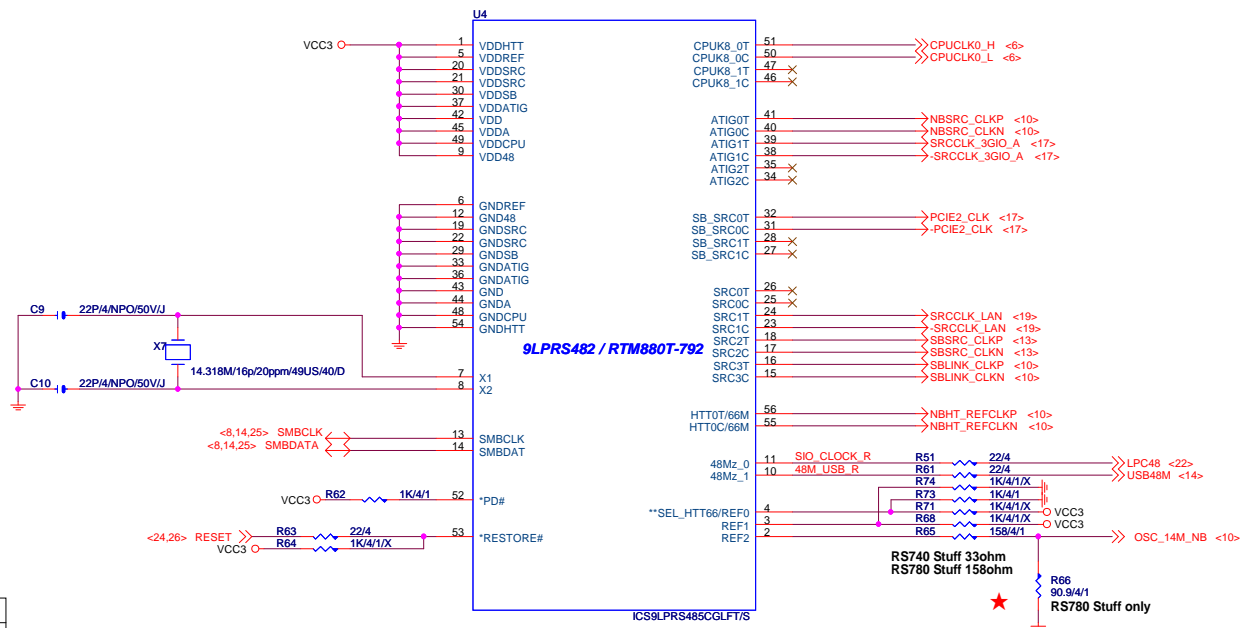


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCLKTx AND SRCCLKx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

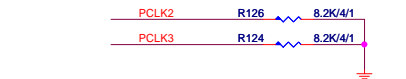
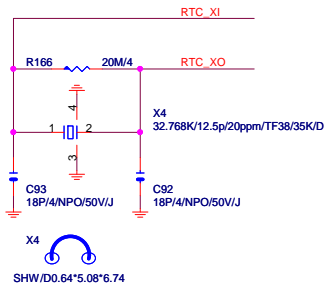
**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.



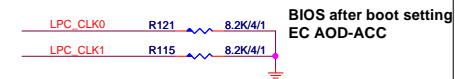
A diagram of a square with vertices labeled 1, 2, 3, 4. The label **SB\_HS** is placed near the top-left vertex (1).

[illegible]

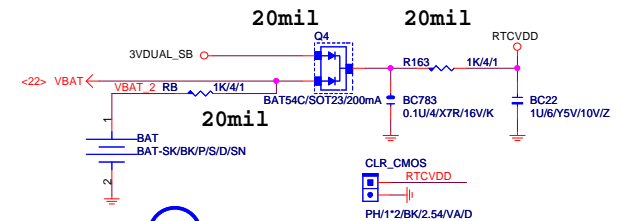
Note: LDT\_PG, LDT\_STP# & LDT\_RST# are ODRs and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT



	LPC_CLK0	LPC_CLK1
<b>PULL HIGH</b>	IMC ENABLED	CLKGEN ENABLED
<b>PULL LOW</b>	IMC DISABLED AOD Extreme DEFAULT	CLKGEN DISABLED DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**

**GIGABYTE™**

Title	ATI SB710 PCIE/PCI/CPU/LPC
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Size Custom	Document Number <b>GA-78LMT-S2P</b>	Rev <b>4.0</b>
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SLP\_S5 R229 8.2K/4/X  
SB\_TEST2 R69 8.2K/4/1  
SB\_TEST1 R70 8.2K/4/1  
SB\_TEST0 R72 8.2K/4/1

SUS\_STAT R208 8.2K/4/1  
SMBCLK R78 1K/4/1  
SMBDATA R79 1K/4/1  
WD\_PWRGD R61 8.2K/4/1

RI R187 8.2K/4/1  
SMBCLK1 R173 2.2K/4/1  
SMBDATA1 R181 2.2K/4/1  
PCIPME R209 2.2K/4/1  
PCIE\_WAKE R211 2.2K/4/1

SB\_PWROK C1064 100P/4/NPO/50V/X

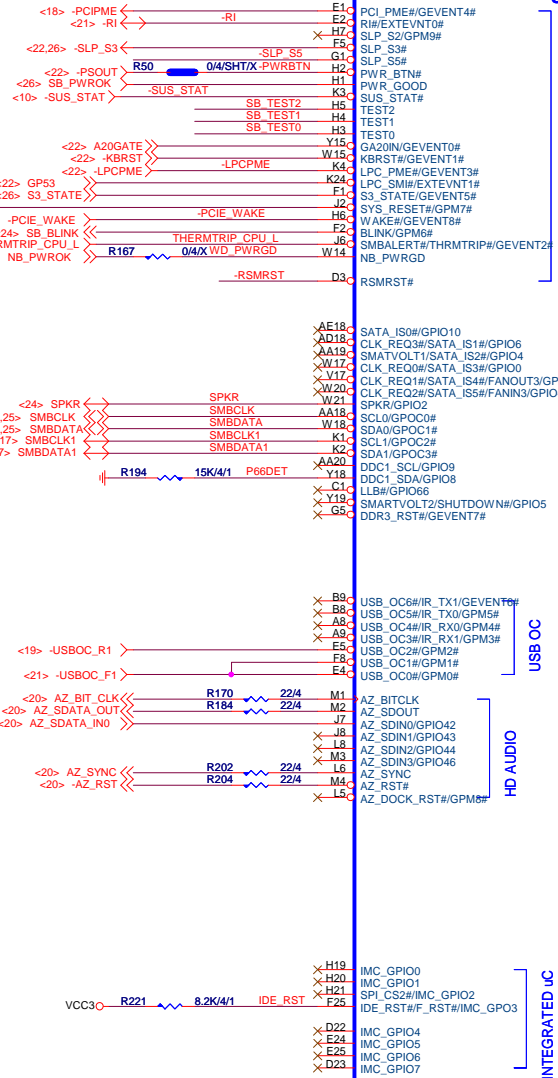
SMBCLK1 C1052 100P/4/N/50V/X  
SMBDATA1 C1053 100P/4/N/50V/X

AZ\_BIT\_CLK C1063 22P/4/NPO/50V/X

AZ\_RST R77 8.2K/4/1

3VDUAL\_SB R82 20K/4/1  
BC28 2.2u/8/X5R/10V/K

AZ\_RST#  
PULL ENABLE PCI  
HIGH MEM BOOT  
PULL DISABLE PCI  
LOW MEM BOOT  
DEFAULT



SB700

Part 4 of 5

USB11 FRONT PANEL  
USB10 FRONT PANEL  
USB9 FRONT PANEL  
USB8 FRONT PANEL  
USB7 FRONT PANEL  
USB6 FRONT PANEL  
USB5 FRONT PANEL  
USB4 FRONT PANEL  
USB3 REAR PANEL  
USB2 REAR PANEL  
USB1 REAR PANEL  
USB0 REAR PANEL

either HWM inputs or PWR\_GD signals  
can be used for power-up sequencer

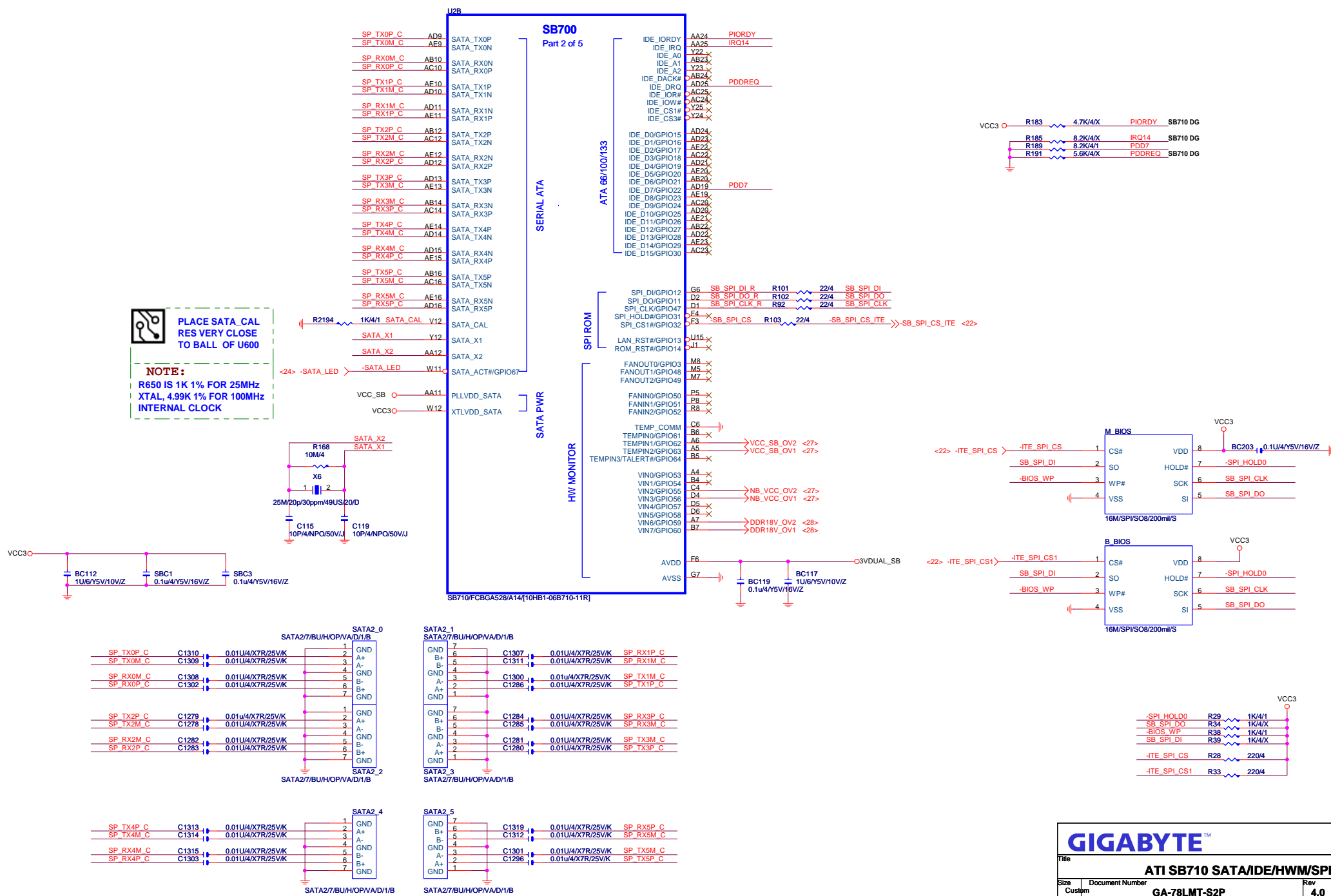
IMC\_GPIO17 R112 2.2K/4/1  
IMC\_GPIO16 R83 2.2K/4/1

ROM TYPE:  
H, H = Reserved  
H, L = SPI ROM DEFAULT  
L, H = LPC ROM  
L, L = FWB ROM

VCC18 R259 8.2K/4/1  
IMC\_TDO  
CPU\_TDI CPU\_TDI <6>

VCC18 R287 8.2K/4/1  
IMC\_TMS  
CPU\_TMS CPU\_TMS <6>

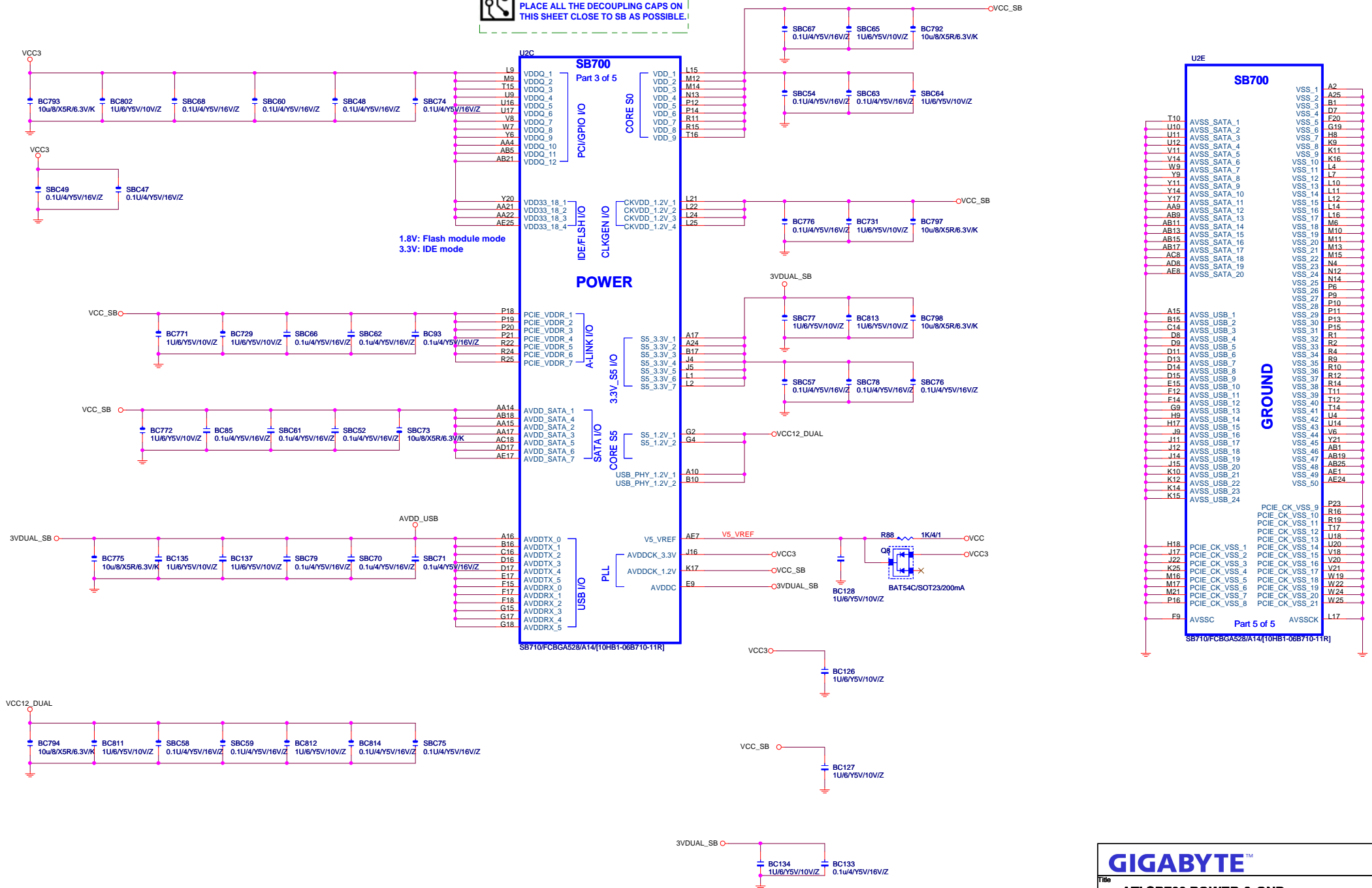
VCC18 R290 8.2K/4/1  
IMC\_TCK  
CPU\_TCK CPU\_TCK <6>



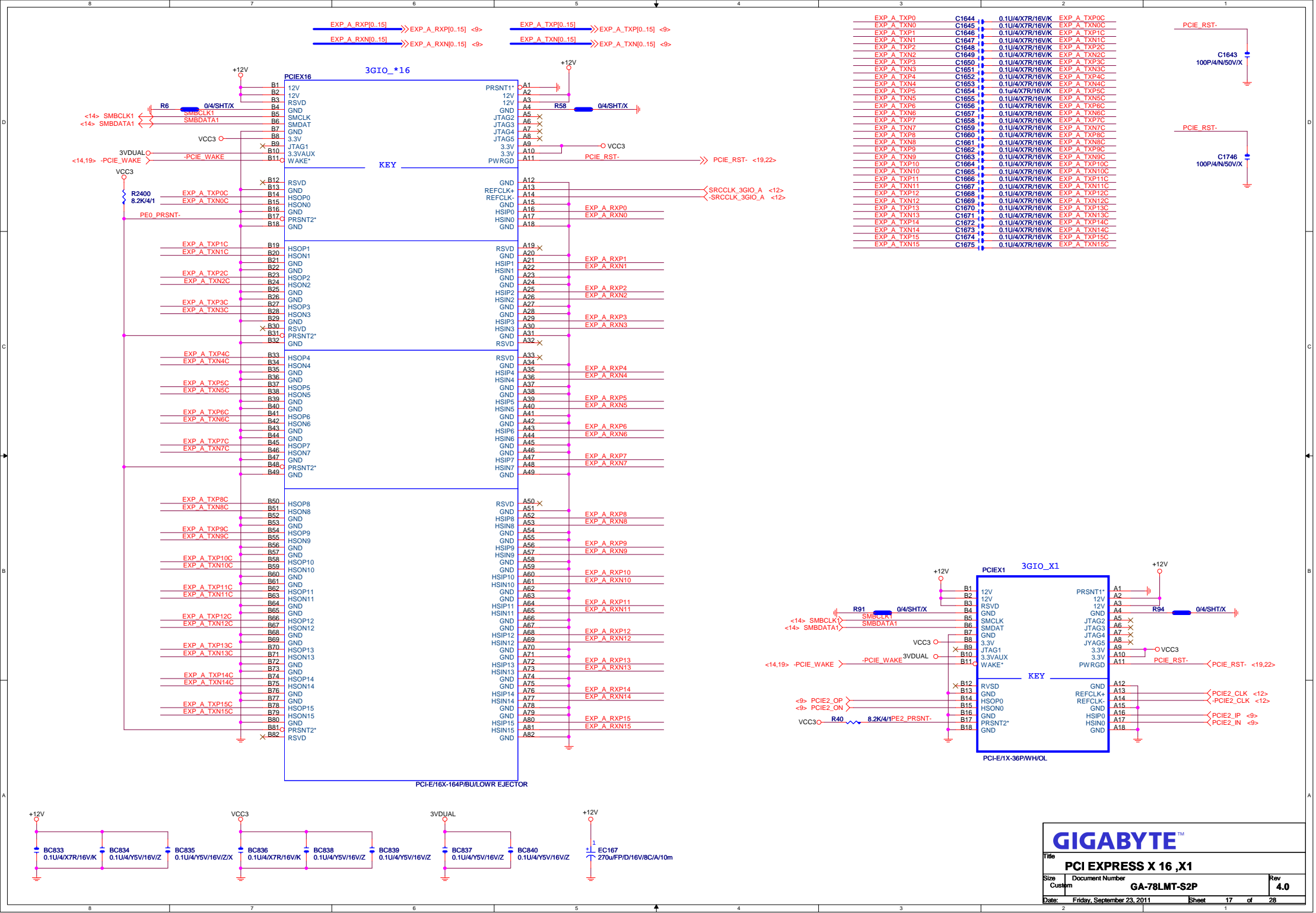




PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

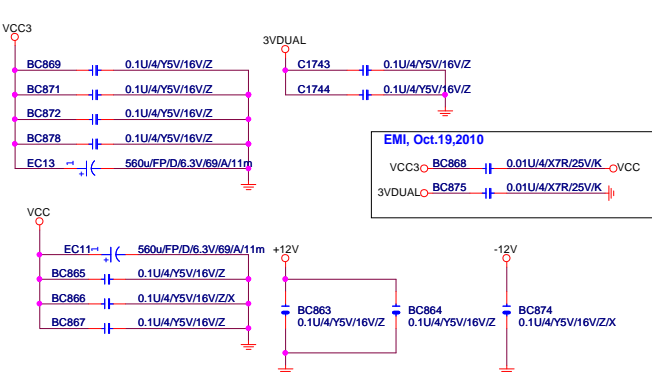
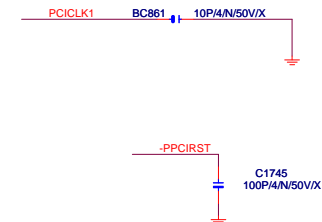
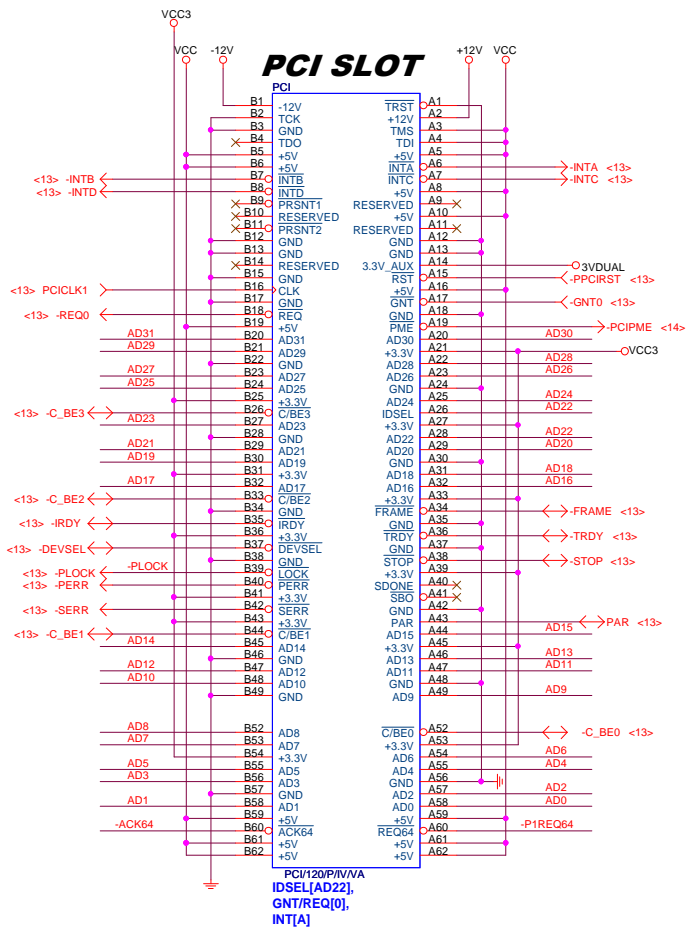






# PCI SLOT 1,2

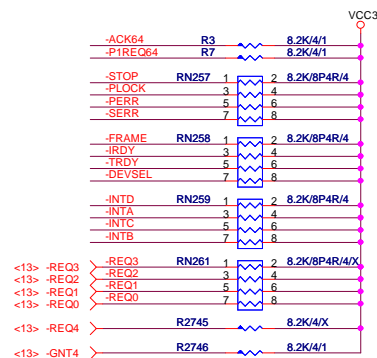
<13> AD[0..31] <-> AD[0..31]



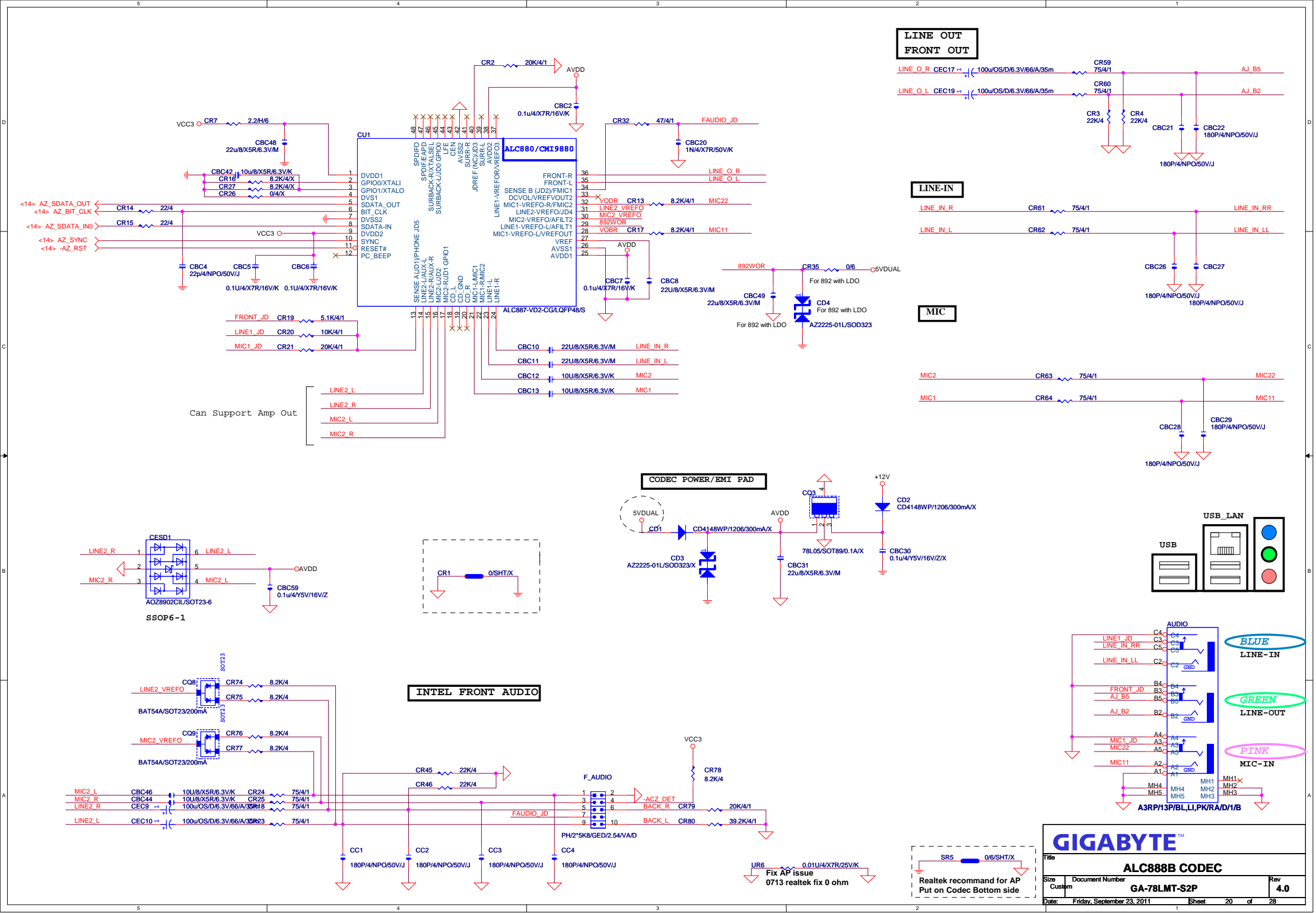
**EMI, Oct.19,2010**

VCC3 <-> BC868 <-> 0.01U/4/X7R/25V/K <-> VCC

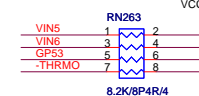
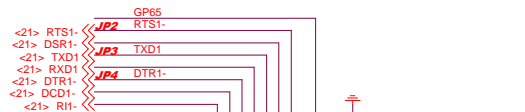
3VDUAL <-> BC875 <-> 0.01U/4/X7R/25V/K <->



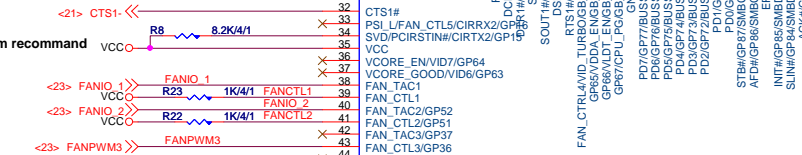




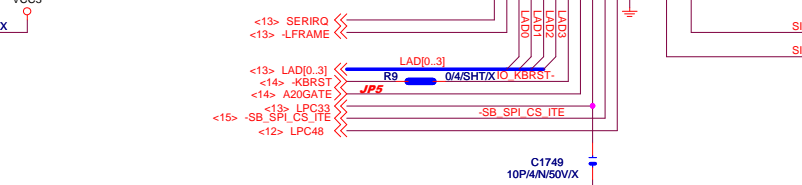
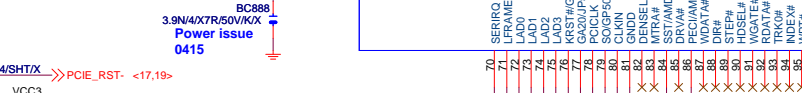
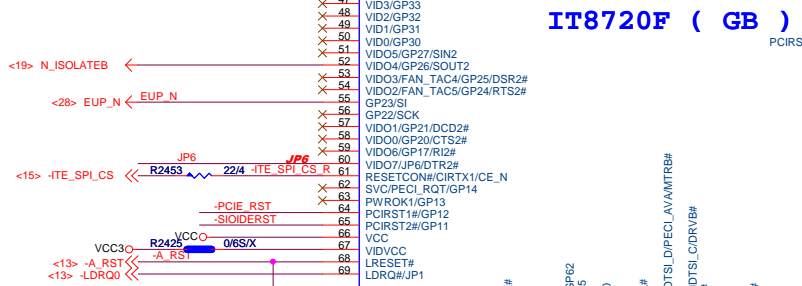




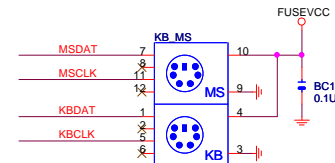
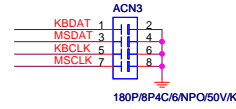
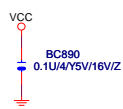
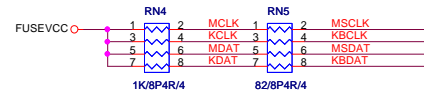
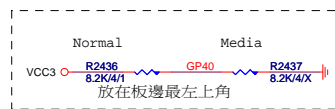
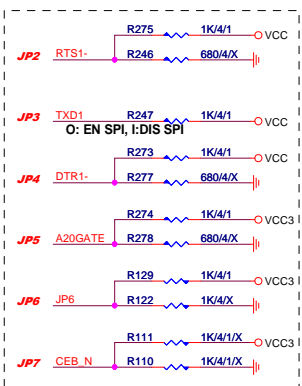
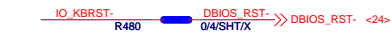
ITE Tom recommend



IT8720F ( GB )



Symbol	value	Description
JP1		
Pin 69		
JP2		
Pin 25		
JP3		
Pin 27		
JP4		
Pin 29		
JP3 & JP5		
Pin 27 & Pin 77		
JP5		
Pin 77		
JP6		
Pin 60		
JP7		
Pin 97		



KB/MS/6P/CP99/OS/RA/D2/[11NR6-802006-19R\_11NR6-802006-1ER]

ITE 8720 LPC IO

Size: Custom

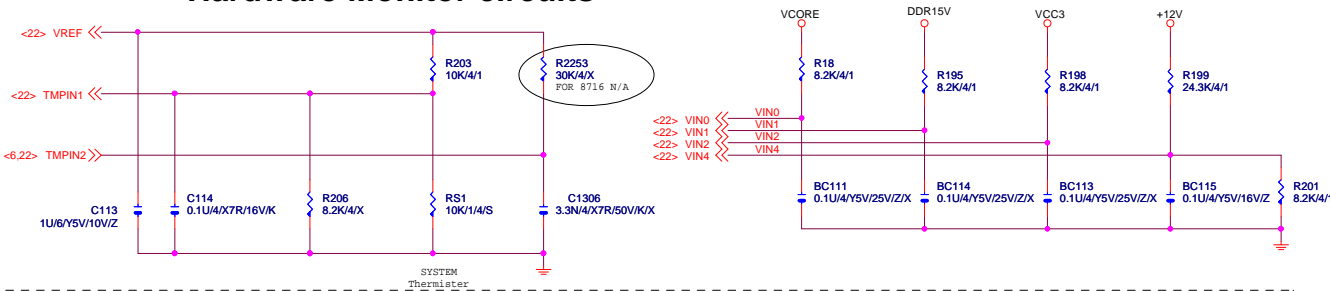
Document Number: GA-78LMT-S2P

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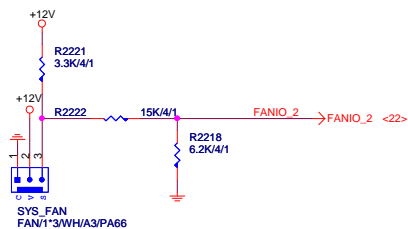
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Rev: 4.0

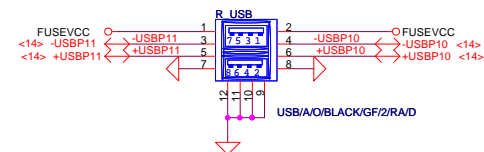
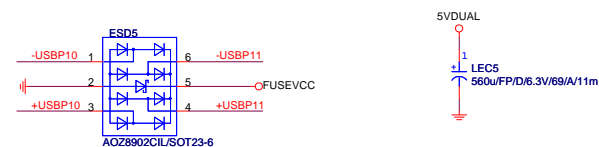
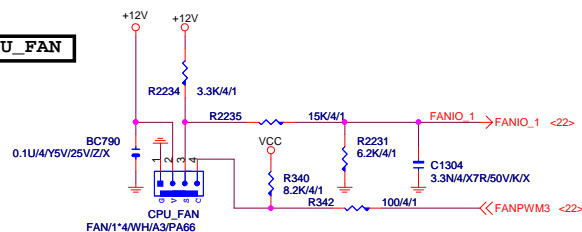
# Hardware Monitor circuits

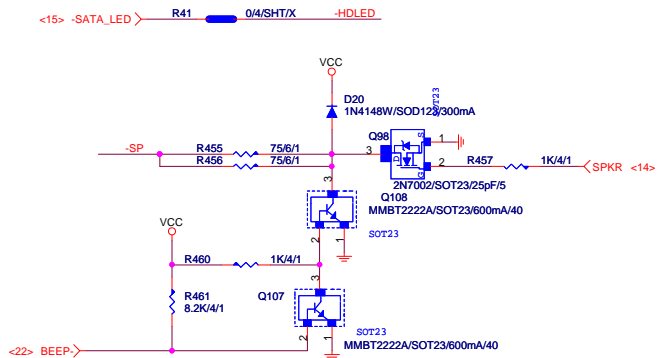
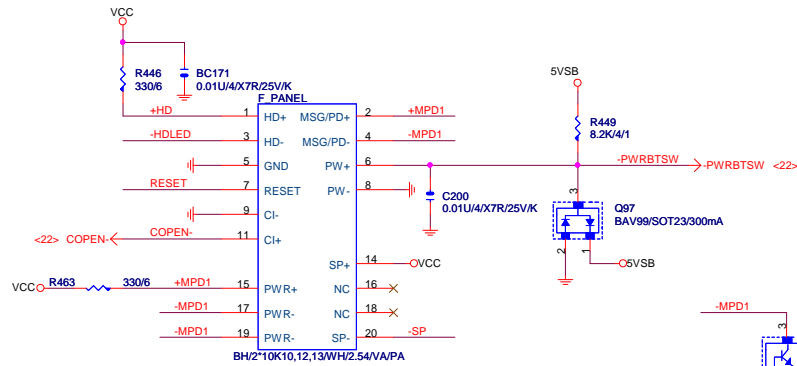


## SYSTEM FAN

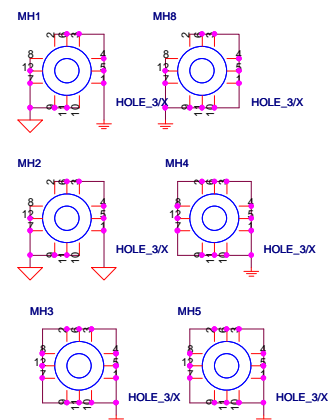
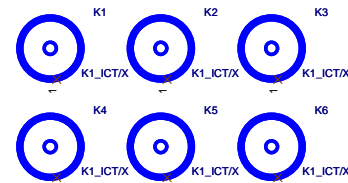
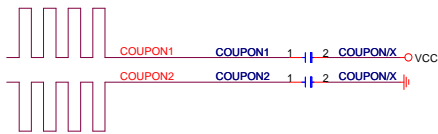
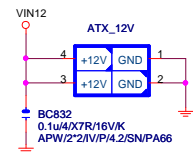
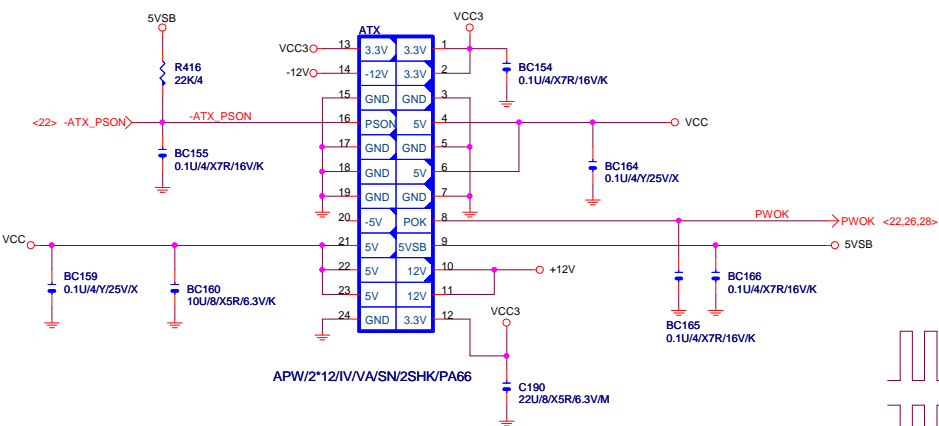


## CPU\_FAN





## ATX POWER CONNECTOR



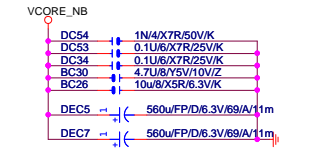
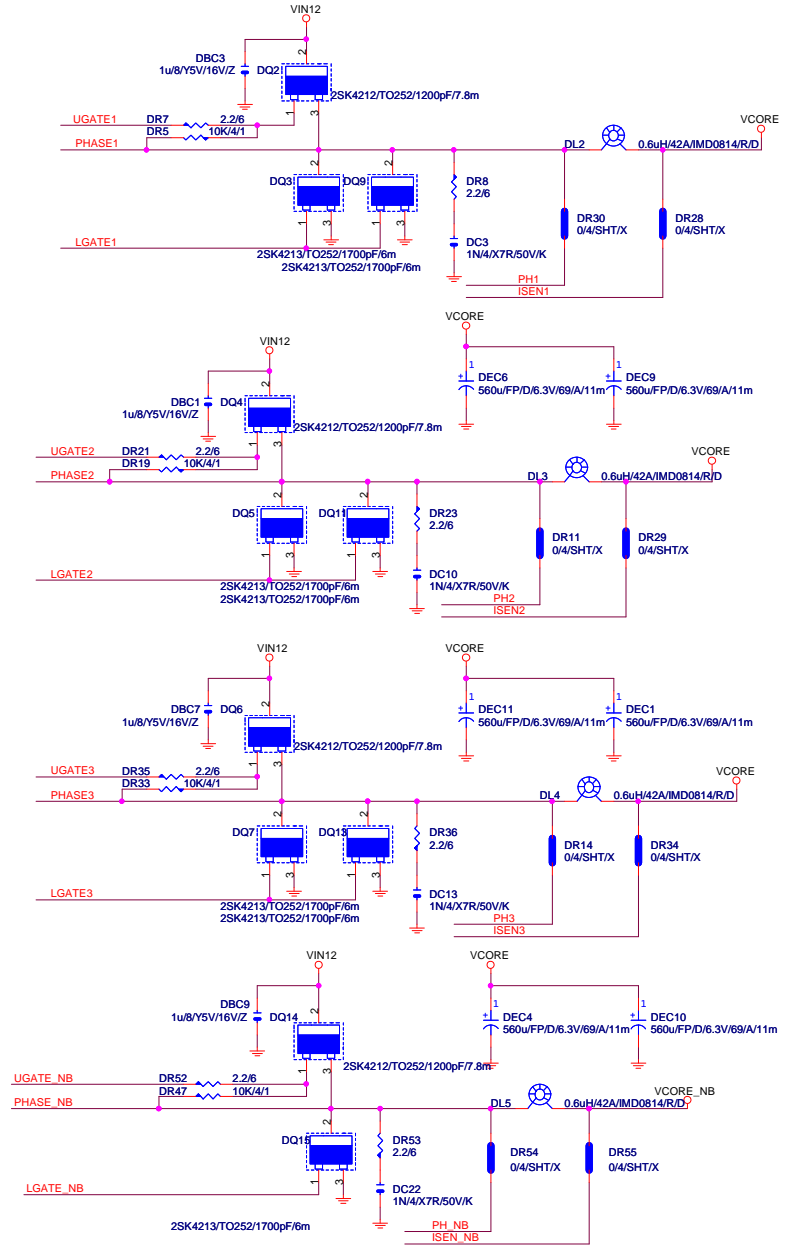
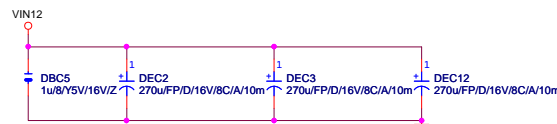
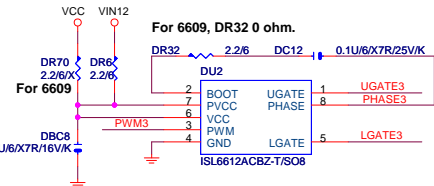
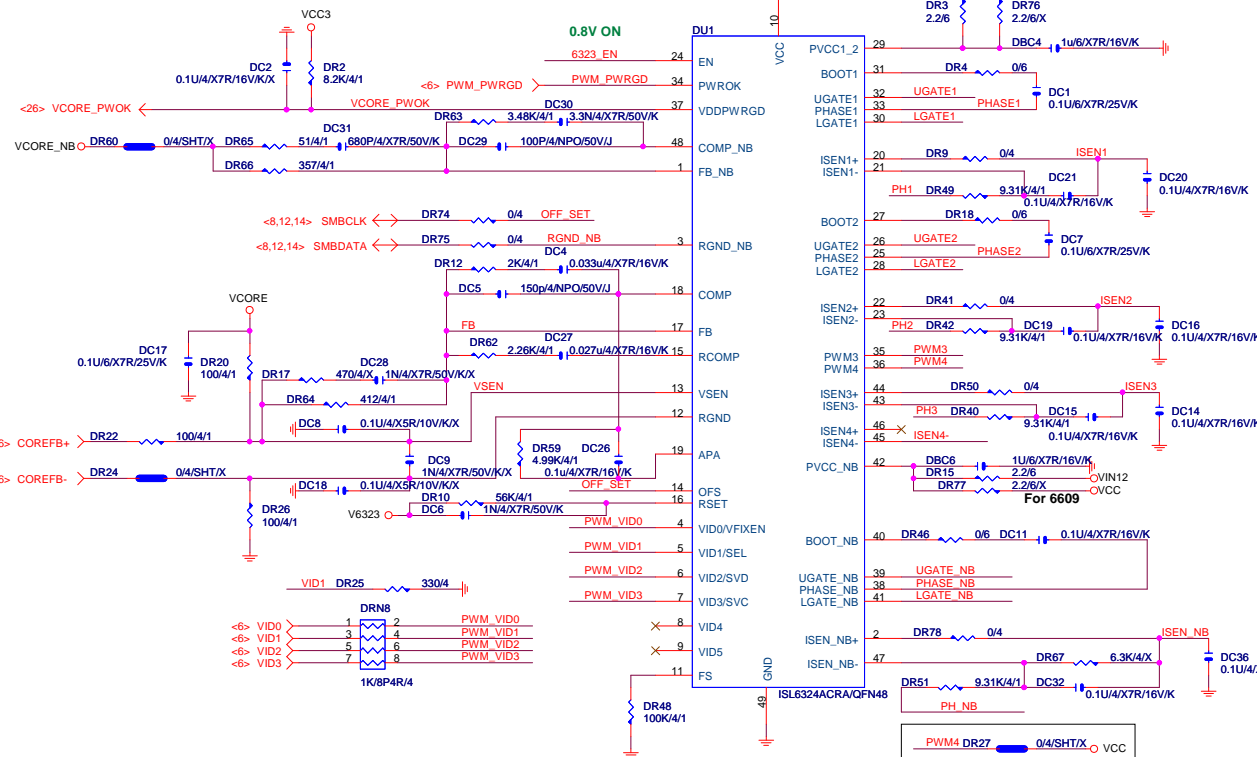


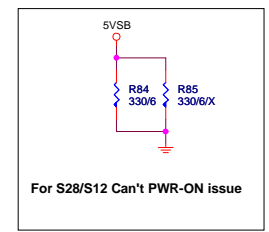
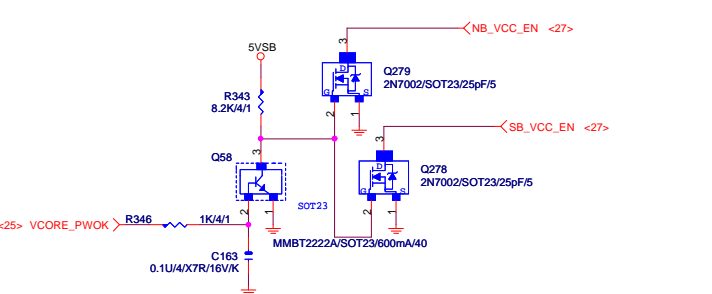
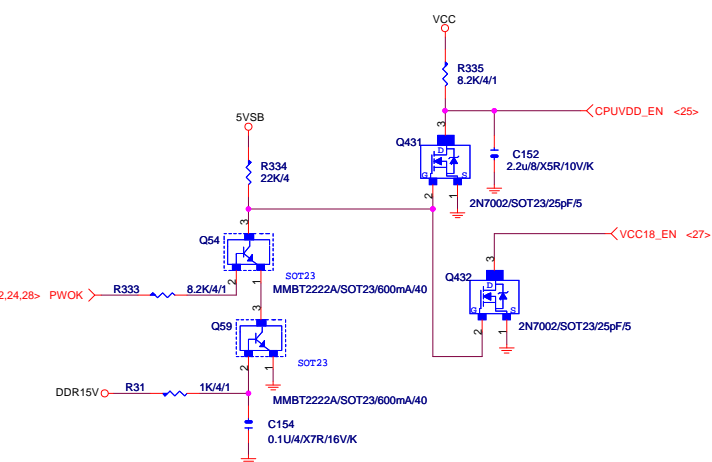
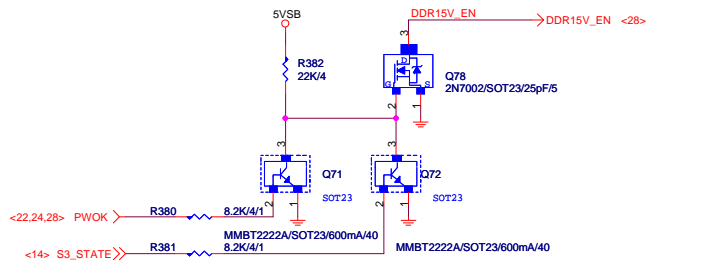
<26> CPUVDD\_EN CPUVDD\_EN DR1 0/4/SHT/X 6323\_EN

PWROK (SVI)  
Low : "metal VID"  
High : running protocol

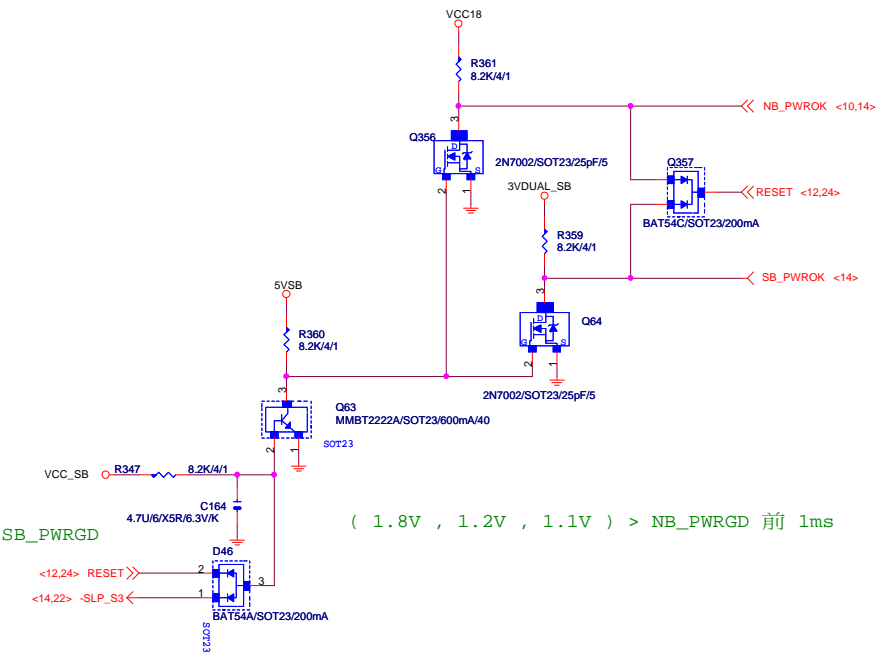
EN rising edge :  
Hi : PVI mode  
Low : SVI mode

Pin 34 Input, Pin 37 Output

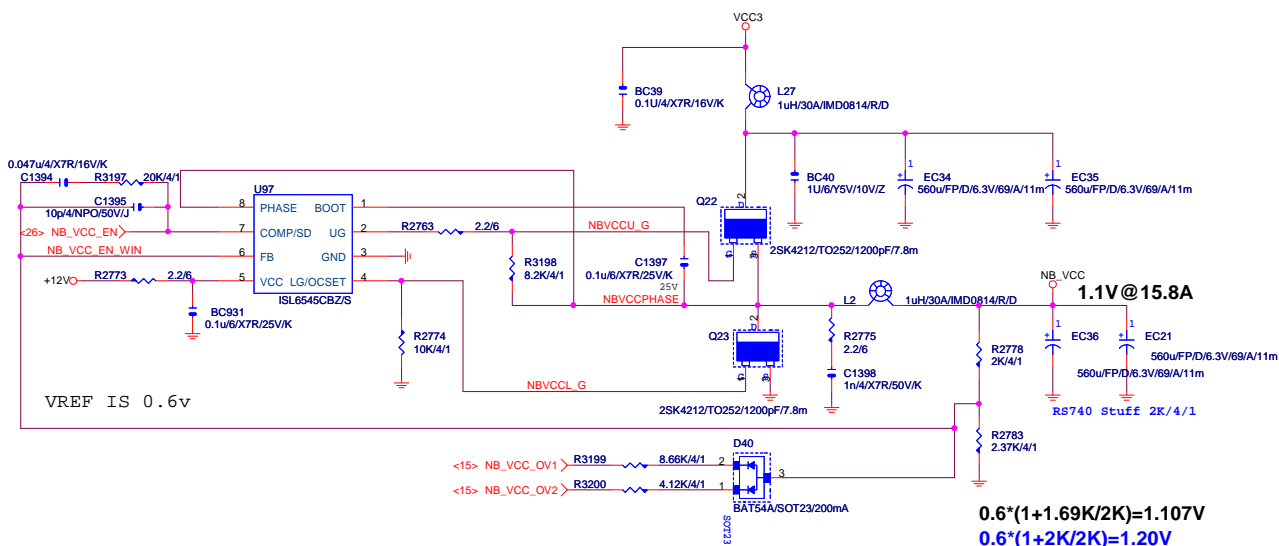




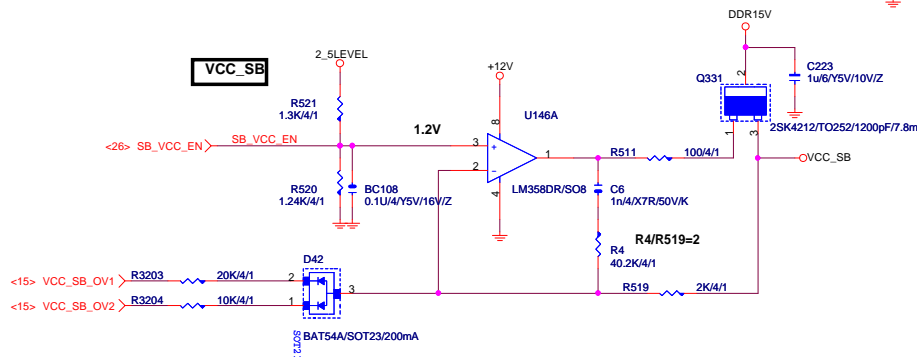
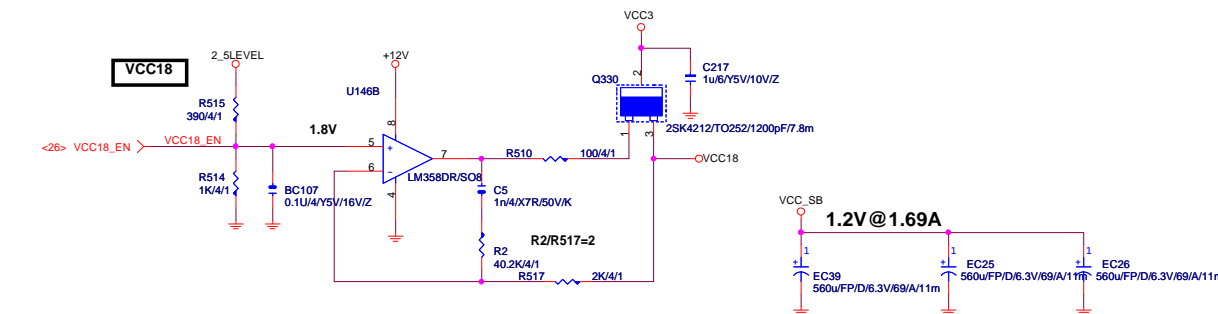
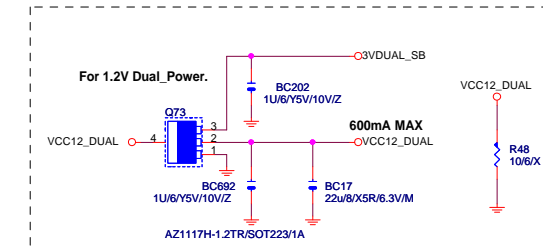
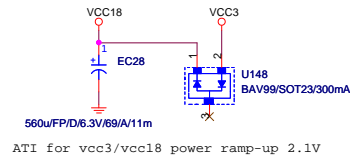
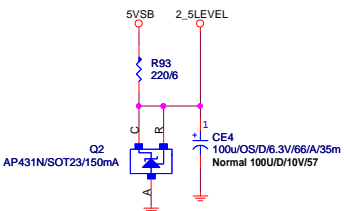
PWOK > NB\_PWRGD / SB\_PWRGD



( 1.8V , 1.2V , 1.1V ) > NB\_PWRGD 前 1ms



NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V



VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

